

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Houston	Docket No.: TI-31245
Serial No: TBD	Examiner: TBD
Filed: 10/25/01	Art Unit: TBD
For: METHOD AND APPARATUS FOR REDUCING CAPACITIVE COUPLING BETWEEN LINES IN AN INTEGRATED CIRCUIT	



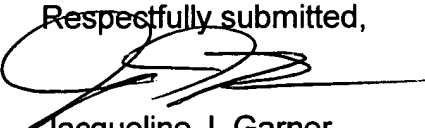
**INFORMATION DISCLOSURE STATEMENT**

Assistant Commissioner for Patents  
Washington, DC 20231

Dear Sir:

Please make the references listed on the enclosed PTO-1449 of record under 37 C.F.R. 1.56, 1.97, and 1.98 in the patent application identified above. Copies of the listed references are enclosed.

Respectfully submitted,

  
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FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

TI-31245

SERIAL NO.

TBD

## LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

APPLICANT

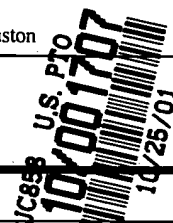
Theodore W. Houston

FILING DATE

10/25/01

GROUP

TBD



## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE (IF APPROPRIATE)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION Yes No
	BA						
	BB						
	BC						
	BD						
	BE						

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	CA	Takeda, et al. "A 16-Mb 400-MHz Loadless CMOS Four-Transistor SRAM Macro", IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1631-1640.
	CB	
	CC	
	CD	
	CE	

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.